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REMARKS

Entry of this Amendment is believed proper since no new issues are being raised which would require the Examiner's further consideration and/or search.

Claims 1-20 are presently pending in this application. Claim 1 has been amended to more particularly define the claimed invention.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by Houssein et al., U.S. Pat. No. 6,418,479.

This rejection is respectfully traversed in view of the following discussion.

I. APPLICANT'S CLAIMED INVENTION

The claimed invention (as defined, for example, by independent claim 1) is directed to a clustered computer system including, a plurality of CPU and memory installed apparatuses having at least one CPU and at least one memory, and a plurality of input/output control apparatuses. The CPU and memory installed apparatuses and the input/output control apparatuses are connected to each other by a network, and the CPU and memory installed apparatuses transmit an input/output instruction to at least one of the plurality of input/output control apparatuses assigned in advance.

Conventionally, the problem of a conventional computer system is that when a CPU or memory of computer system fails and cannot be used, even if input/output control circuit in the faulty computer system is free of any fault and hence is normal, the normal input/output control circuit and peripheral devices under its control cannot be used. The reason for this problem is that in a conventional computer system the input/output control circuit can only be controlled from a CPU that is connected thereto through the control circuit, and the CPU and the input/output control circuit which carries out input/output instructions issued by the CPU are assembled on same board, which is a minimum unit for maintenance and replacement. (Application at page 3, line 23 to page 4, line 10.)

The claimed invention (e.g., as recited in claims 1 and 2), on the other hand, includes *the CPU and memory installed apparatuses transmit an input/output instruction to at least one of the plurality of input/output control apparatuses assigned in advance*. This feature is important increase the availability of a computer system upon a fault thereof. (Application at page 4, lines 11-13.)

II. THE ALLEGED PRIOR ART REJECTION

The Examiner alleges that Houssein et al., U.S. Pat. No. 6,418,479, (Houssein), teaches the invention of claims 1-20.

With respect to Applicant's independent claim 1, Houssein fails to teach or suggest, "*wherein causing said CPU and memory installed apparatuses to transmit an input/output instruction to at least one of said plurality of input/output control apparatuses assigned in advance*."

With respect to Applicant's independent claim 2, Houssein fails to teach or suggest,

"wherein each of said input/output control apparatuses comprises communication means for receiving an input/output instruction from at least one CPU and memory installed apparatuses assigned in advance to at least one of said plurality of input/output control apparatuses via said network, and transmits a response to said input/output instruction to said at least one CPU and memory installed apparatuses via said network."

Houssein fails to teach or suggest *assigning in advance* I/O nodes 230 to respective host nodes 210. Houssein only discloses that "each host node 210 is connected to each I/O node 230 via a network, such as a system area network (SAN) 220." (Column 2, lines 26-28.)

With respect to Applicant's independent claim 13, Houssein fails to teach or suggest, *"a communication cable connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other, wherein said CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by said CPU to said input/output control apparatuses via said communication cable, and receives a response from said input/output control apparatuses via said communication cable, and wherein said input/output control apparatuses comprising communication means for receiving an input/output instruction from said CPU and memory installed apparatuses via said communication cable, and transmits a response to said input/output instruction to said CPU and memory installed apparatuses via said communication cable."*

The Final Office Action cites passages in Houssein that make no mention of any communication cable connecting host nodes 210 to I/O nodes 230, and Houssein fails to teach or suggest a communication cable connecting each host node 210 to each I/O node 230.

With respect to Applicant's independent claim 14, Houssein fails to teach or suggest, *"communication means for communicating with an external circuit comprising an*

input/output control apparatus, transmitting an input/output instruction issued by said CPU to said input/output control apparatuses which has been assigned in advance, and receiving a response from said input/output control apparatus."

Again, Houssein fails to teach or suggest *assigning in advance* I/O nodes 230 to respective host nodes 210. Houssein only discloses that "each host node 210 is connected to each I/O node 230 via a network, such as a system area network (SAN) 220." (Column 2, lines 26-28.)

With respect to Applicant's independent claim 16, Houssein fails to teach or suggest, "*communication means for communicating with an external circuit comprising a CPU and memory installed apparatus, for receiving an input/output instruction from said CPU and memory installed apparatus which has been set in advance and transferring said input/output instruction to said input/output control circuit, and for transmitting a response to said input/output instruction to said CPU and memory installed apparatus.*"

As mentioned above, with respect to independent claims 2 and 14, Houssein fails to teach or suggest *assigning in advance* I/O nodes 230 to respective host nodes 210.

Therefore, Applicant respectfully requests Examiner to reconsider and withdraw this rejection since the alleged prior art reference fails to teach or suggest each and every element and feature of Applicant's claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: Sept. 21, 2006

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CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (571) 273-8300 the enclosed Amendment under 37 C.F.R. § 1.116 to Examiner MARTIN, Art Unit 2157, on September 21, 2006.

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